In the Specification.

Please replace the title beginning at Page 1, Line 1 with the following replacement title.

SEMICONDUCTOR APPARATUS INCLUDING A MULTI-LAYER WIRING CONFIGURATION AND MANUFACTURING METHOD THEREFOR

Please replace the paragraph beginning at Page 4, Line 22 with the following replacement paragraph.

A1

It is noted that in FIG. 6, first wiring layer **M1** is used for interconnect in the vertical direction within a conventional functional circuit block **600**. The second wiring layer **M2** is used for interconnect within the horizontal direction within the conventional function circuit block **600**. This allows a central region **610** to be used for block to block interconnections without the addition of a separate routing channel outside the parameters of the conventional function circuit block **600**.

Please insert the following paragraph at Page 3, line 1.

A2

Referring now to FIG. 7, a conventional memory array is set forth in a block schematic diagram and given the general reference character **700**. Conventional memory array includes capacitor over bit line (COB) memory cells MC connected by a bit line BL.

Please insert the following paragraph at Page 8, line 13.

A3

FIG. 7 is a block schematic diagram of a conventional memory array.

Please replace the paragraph beginning at Page 9, Line 4 with the following replacement paragraph.

As but one example, the material for the second and third wiring layers (**M2** and **M3**) can be aluminum. Aluminum can exhibit approximately a difference of two orders of magnitude lower sheet resistance than the high melting point metal. Although specific values can depend on film thickness, values of the sheet resistance of aluminum can be several tens of mΩ/□ and values of the sheet resistance of a high melting point metal can be several Ω/□.